

# New Transistors for 2005 and Beyond

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Updated information on the TeraHertz transistor  
is available in the 90nm process documents on  
<http://www.intel.com/research/silicon/micron.htm>



# Presentation Topics

- **Technology Goals:**
  - What are Intel's transistor technology goals?
  - How has Intel achieved historical technology goals
- **Transistor Basics:**
  - What is a transistor and how does it work?
  - What are some of the critical performance metrics?
- **Challenges:**
  - What are some of the challenges of the next generation of transistors?
- **Solutions:**
  - How is Intel achieving next-generation goals?

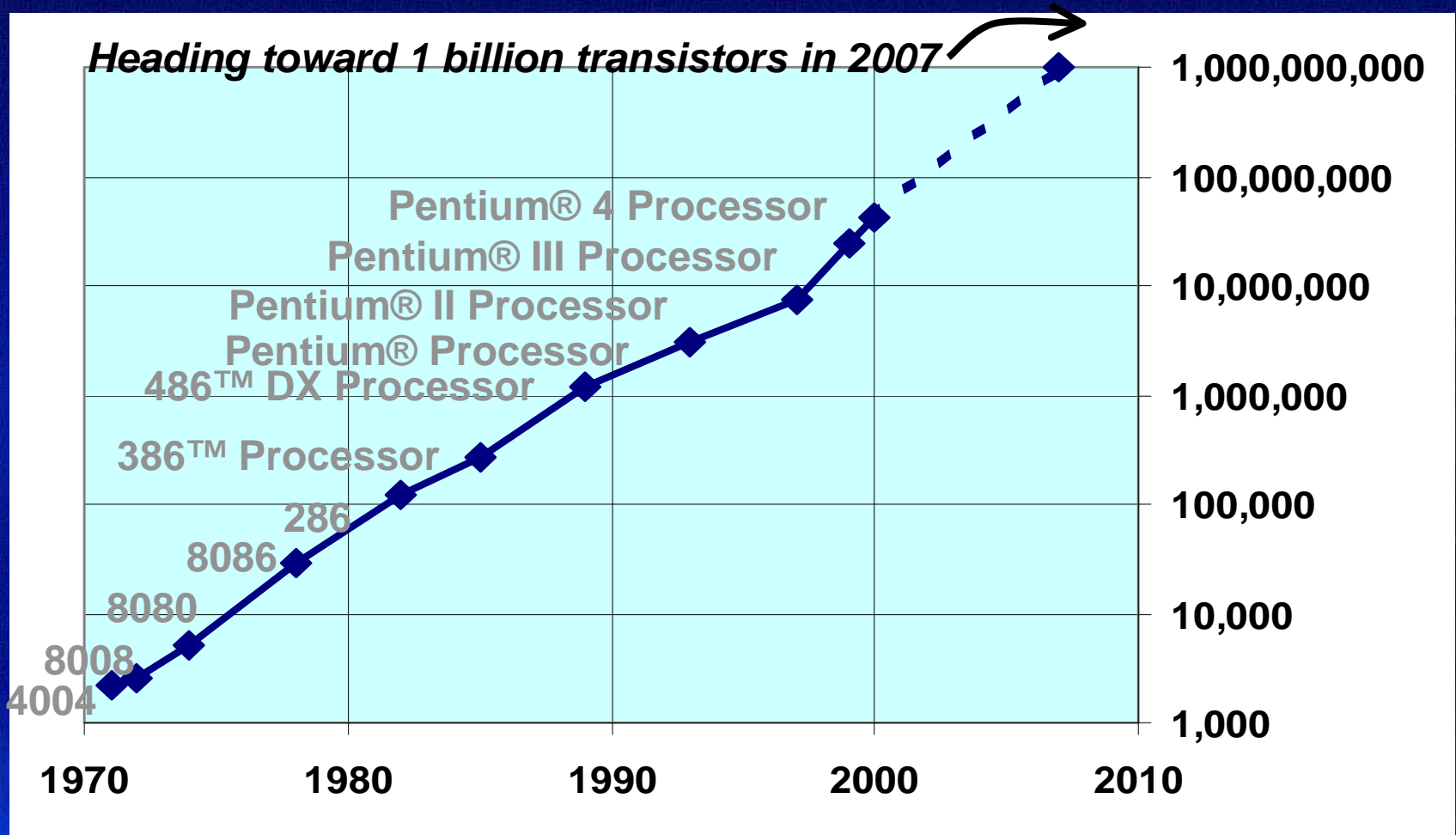


# Moore's Law

- Doubling of number of transistors per integrated circuit every 18-24 months
  - First observed in 1965
- This expectation has driven our research, development, and investments for the last 3 decades
  - Has enabled the incredible progress of the electronics industry

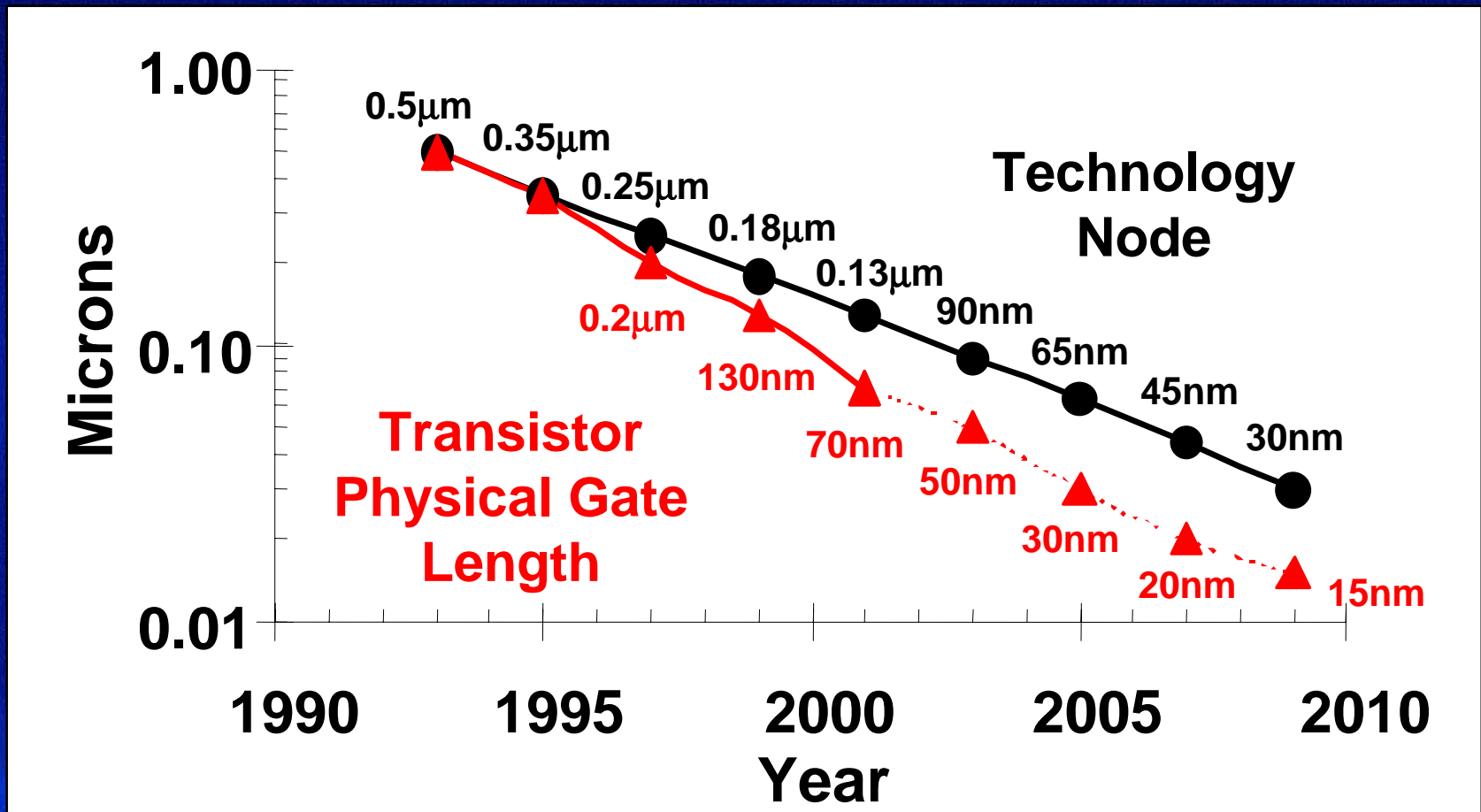
# Moore's Law Continues

Transistors doubling every 2 years toward the billion-transistor microprocessor





# Transistor Physical Gate Length Trend (Lithography generation > $L_{\text{GATE}}$ )



# Transistor progress has accelerated...

## **IEDM: December 2000**

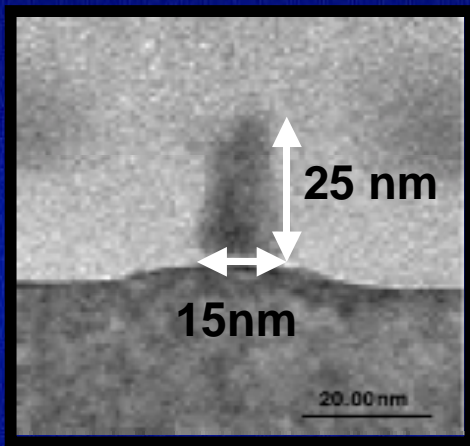
- 30nm gate CMOS; 0.8 nm oxides
- 1.2 THz at 0.85V
- Acceptable short-channel effects, junction leakage and gate leakage.

## **Silicon Nanotechnology Conference: June 2001**

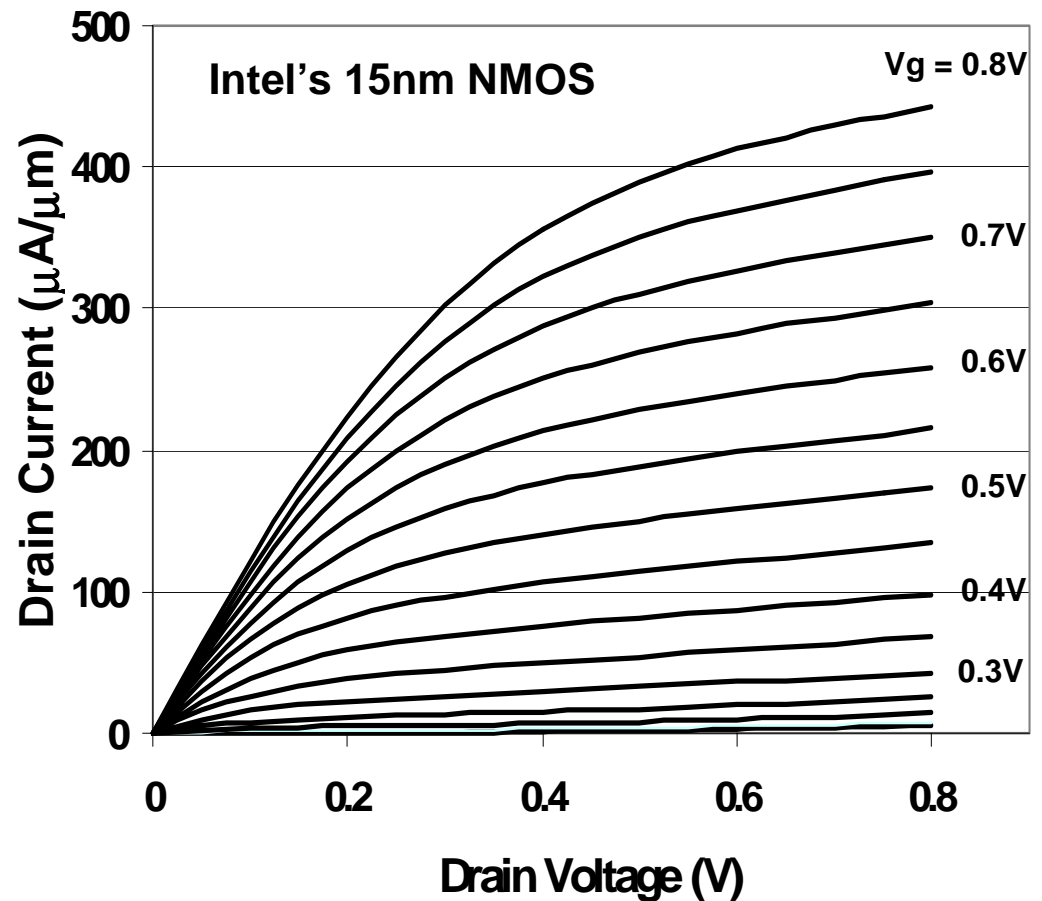
- 20nm gate NMOS
- 1.45 THz at 0.75V



# Yet another record: Intel's 15nm NMOS Transistor



**2.63 THz gate delay  
@ 0.8V!**



# Moore's Law is Driven by Lithography

- 1960's
- 1970's
- 1980's
- 1990's
- 2000's
- Contact printing
- Projection printing
- Wafer steppers, 436nm
- Wafer scanners, 365nm, 248nm
- 193nm, 157nm, EUV ...



# Moore's Law is Driven by New Materials

- 1960's
  - Si, Al, SiO<sub>2</sub>
- 1970's
  - Polysilicon, PSG, Al-Si, Si<sub>3</sub>N<sub>4</sub>
- 1980's
  - BPSG, WSi<sub>2</sub>, Polyimide, SOG, PECVD  
SiN, Ti, TiN
- 1990's
  - Al-Cu, W, MoSi<sub>2</sub>, SiOF, Cu,  
C4 package, Si-Ge, Low K ILD
- 2000's
  - High K gate, .....



# Moore's Law is Driven by New Structures

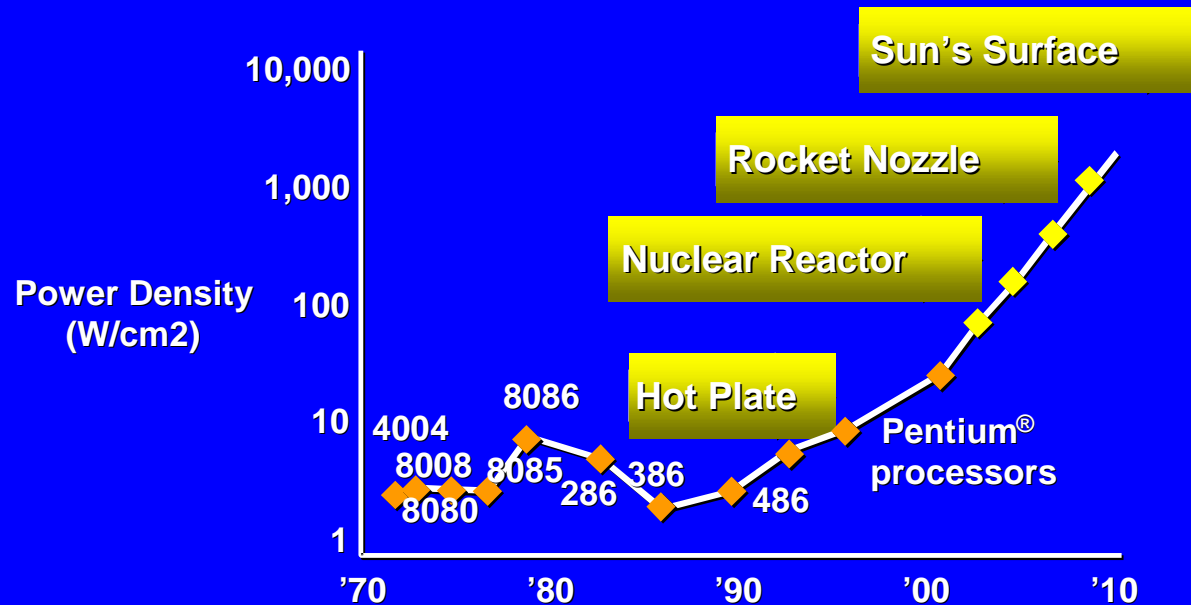
- 1960's
  - Bipolar, Mesa, Metal gate
- 1970's
  - MOS, Polysilicon gate, Locos isolation
- 1980's
  - CMOS, double metal, W plugs, salicide gates
- 1990's
  - STI isolation, Bi-CMOS, CMP, Multi-level metal, Si-Ge Bipolar
- 2000's
  - TeraHertz transistor...



# What's the Problem?

- Power consumption starting to rise exponentially
- Driven by:
  - Transistor  $I_{OFF}$  Leakage
  - Transistor Gate Leakage
  - High Operating Voltage

# Power Density Extrapolation



Gelsinger's Slide from ISSCC 2001



# Fundamental Challenge for This Decade

- Continue Moore's Law without Exponential increase in Power Consumption
- Intel is introducing two important technologies at IEDM :

Depleted substrate transistors

High K gate dielectric

- Our long term approach is:

**TeraHertz Transistors**



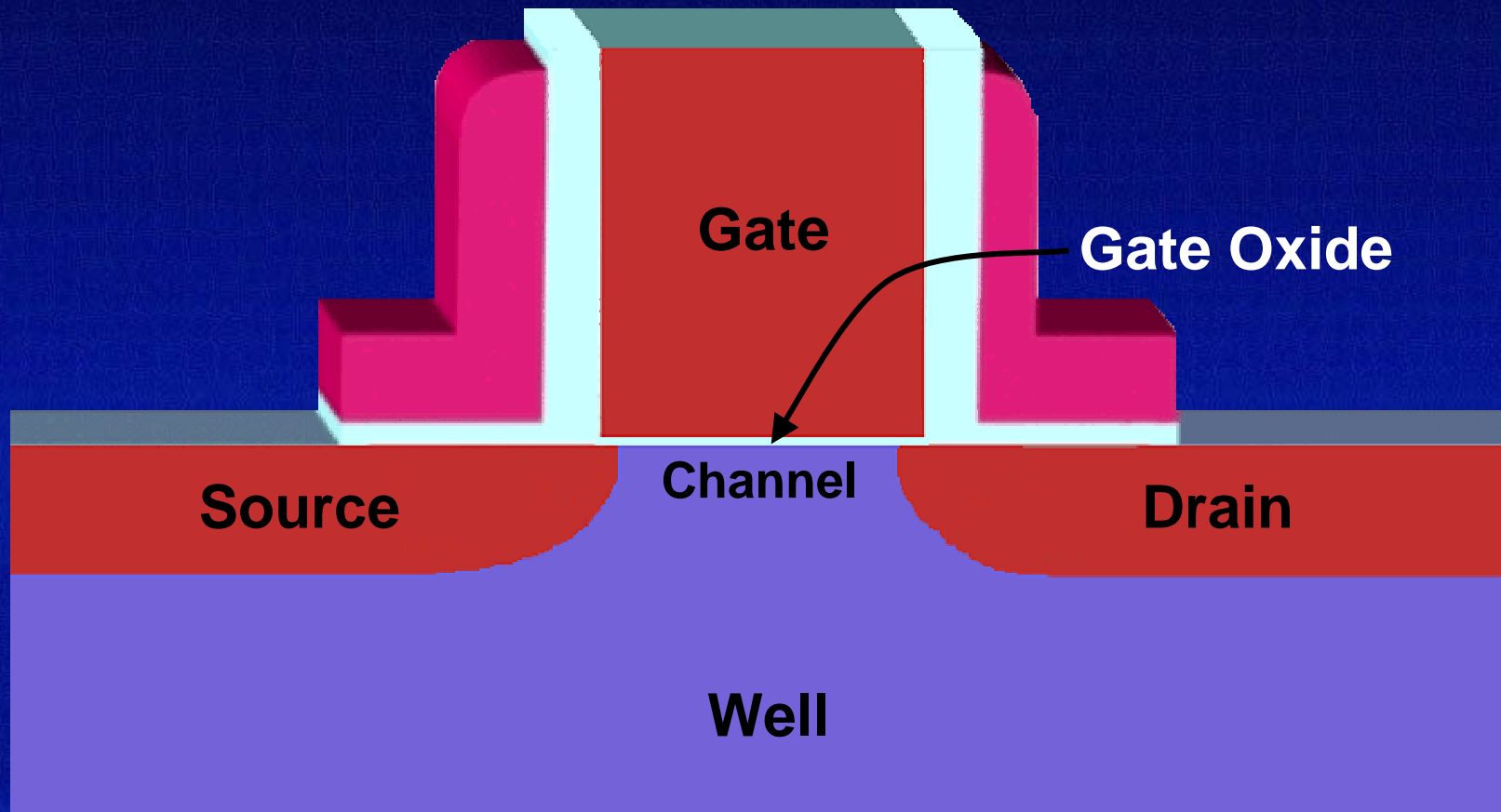
# What is a TeraHertz?

- **Scientific Notation for big**
  - Kilo (thousand)
  - Mega ( million)
  - Giga ( billion)
  - Tera ( trillion)
- **Scientific notation for small**
  - Milli ( thousandth)
  - Micro ( millionth)
  - Nano ( billionth)
  - Pico ( trillionth)

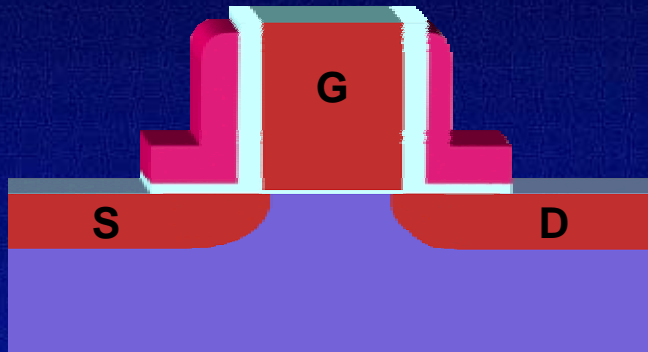
**A TeraHertz transistor will run at 1 trillion cycles per second**



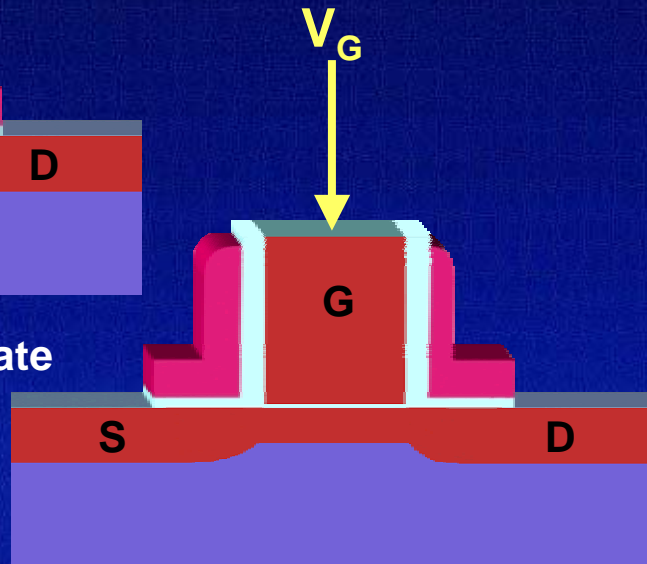
# What is a MOS transistor?



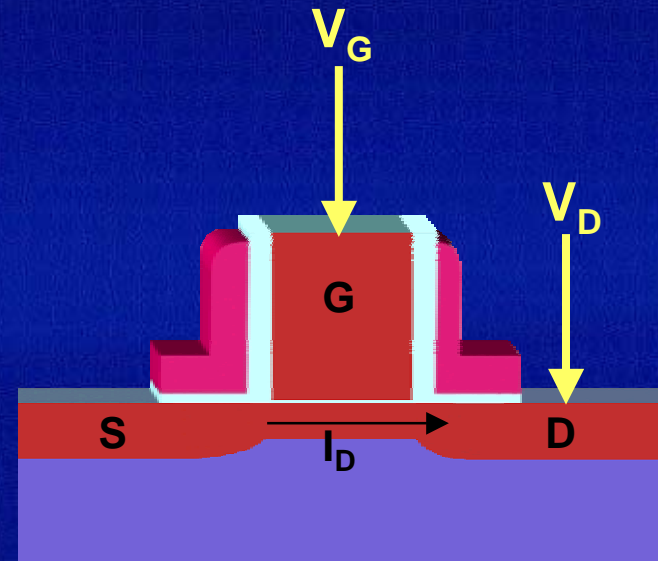
# How does a MOS transistor work?



1. Transistor in “off” state



2. Applying a voltage ( $V_T$ ) to the gate “inverts” the channel region, creating an electrical path between the source and drain



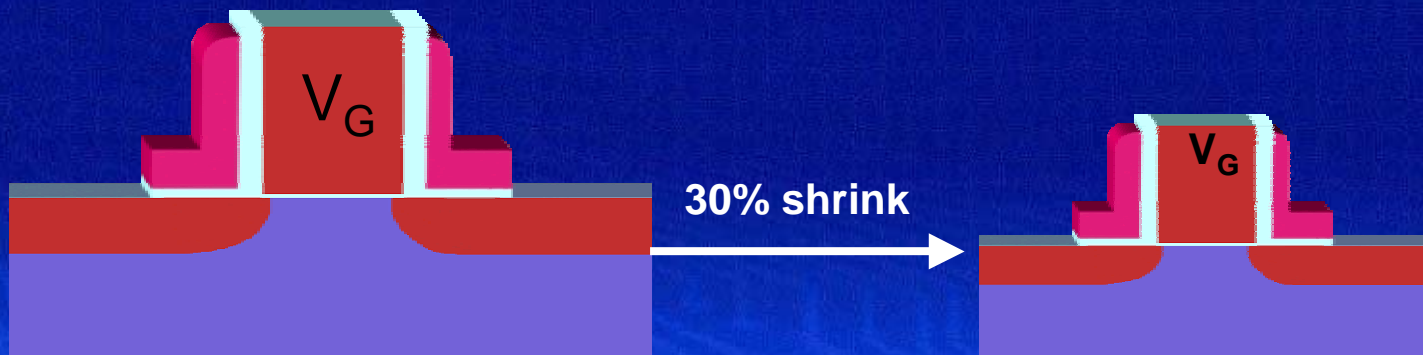
3. Applying a voltage to the drain pulls current-carriers across the channel, creating the drive current ( $I_D$ ).



# Transistor Scaling

- The goal is to create smaller and faster transistors while retaining high level of performance.
- 30% linear shrink yields  $\frac{1}{2}$  transistor area

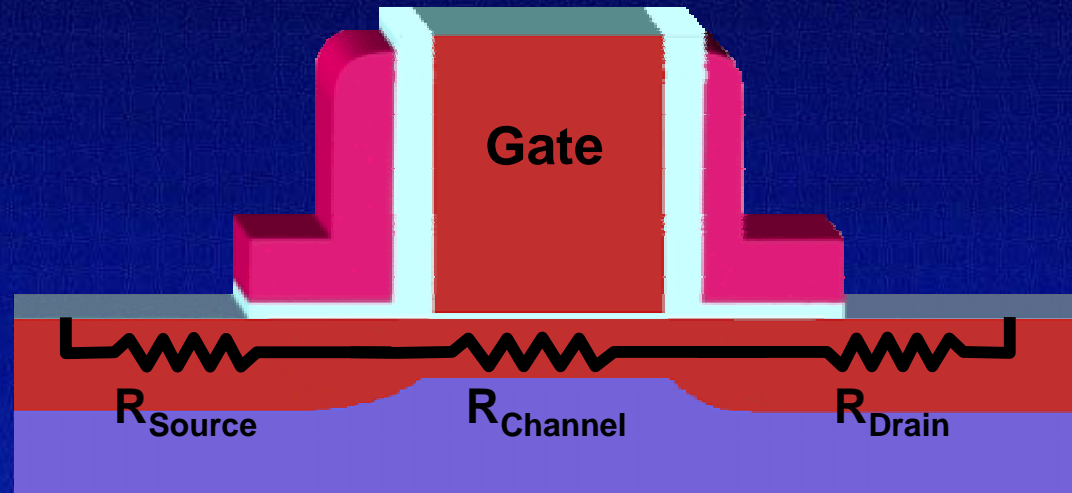
Transistor count doubles every two years



# Source/Drain Resistance

## Resistance

When source/drains have high resistance, higher voltages are needed to move current carriers

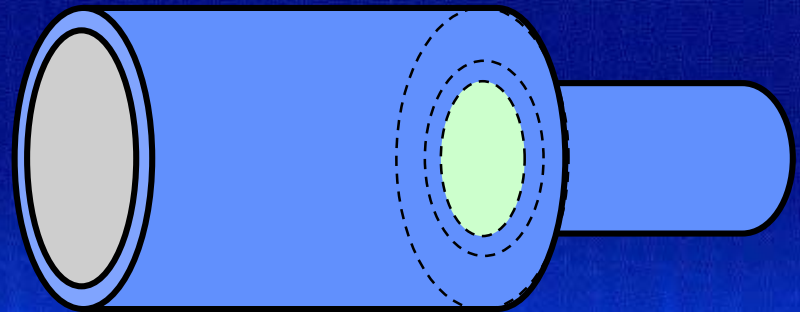


## Resistance: Analogy

Consider forcing water through the following pipes...



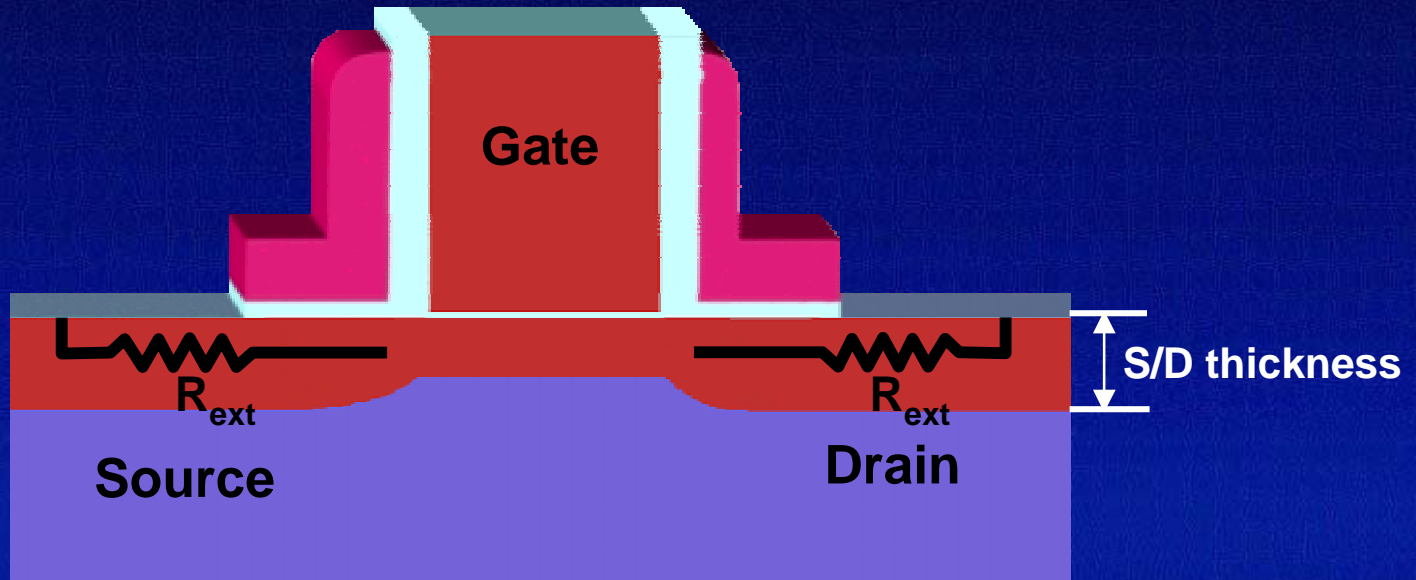
Lower resistance: Large pipe



Higher resistance: pipe has an abrupt change in diameter



# Resistance Challenges



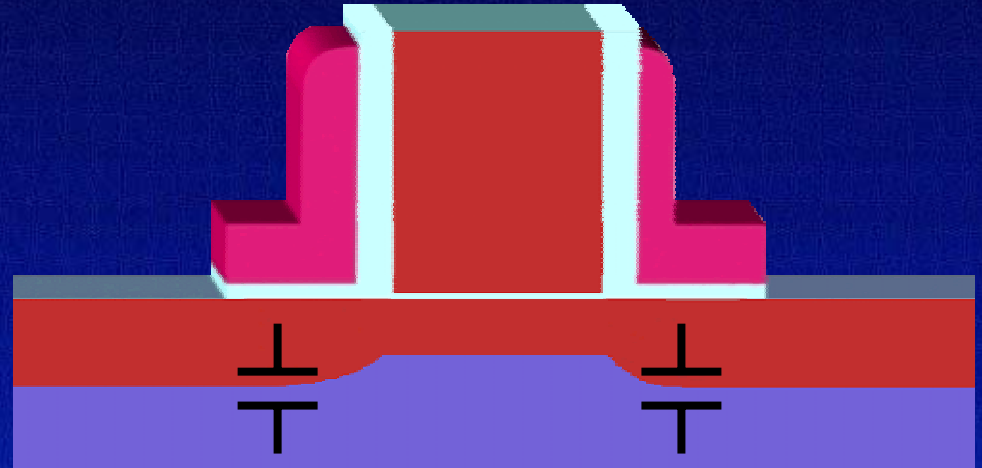
## Resistance: Challenges

- Thinner source and drains have more resistance.
  - Current “crowds” through thin source/drain regions.
- Silicon doping density is at its saturation limit
  - We can’t lower the resistivity

# Source/Drain Junction Capacitance

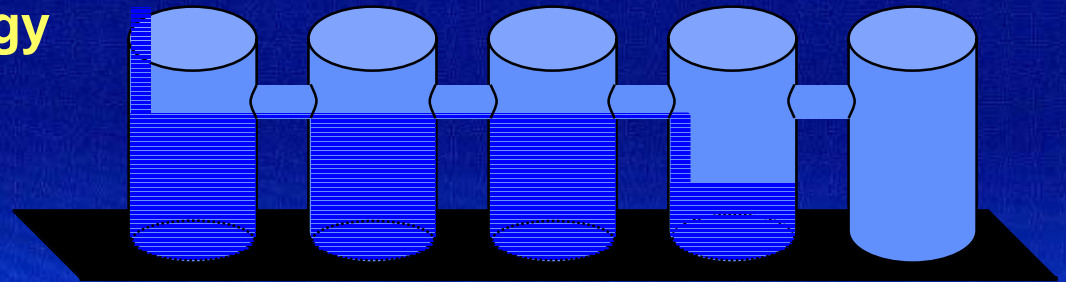
## Capacitance

A high source/drain junction capacitance takes longer for the transistor to build up enough energy to switch on and off.



## Capacitance: Circuit Analogy

Consider filling the final reservoir in a series of reservoirs...

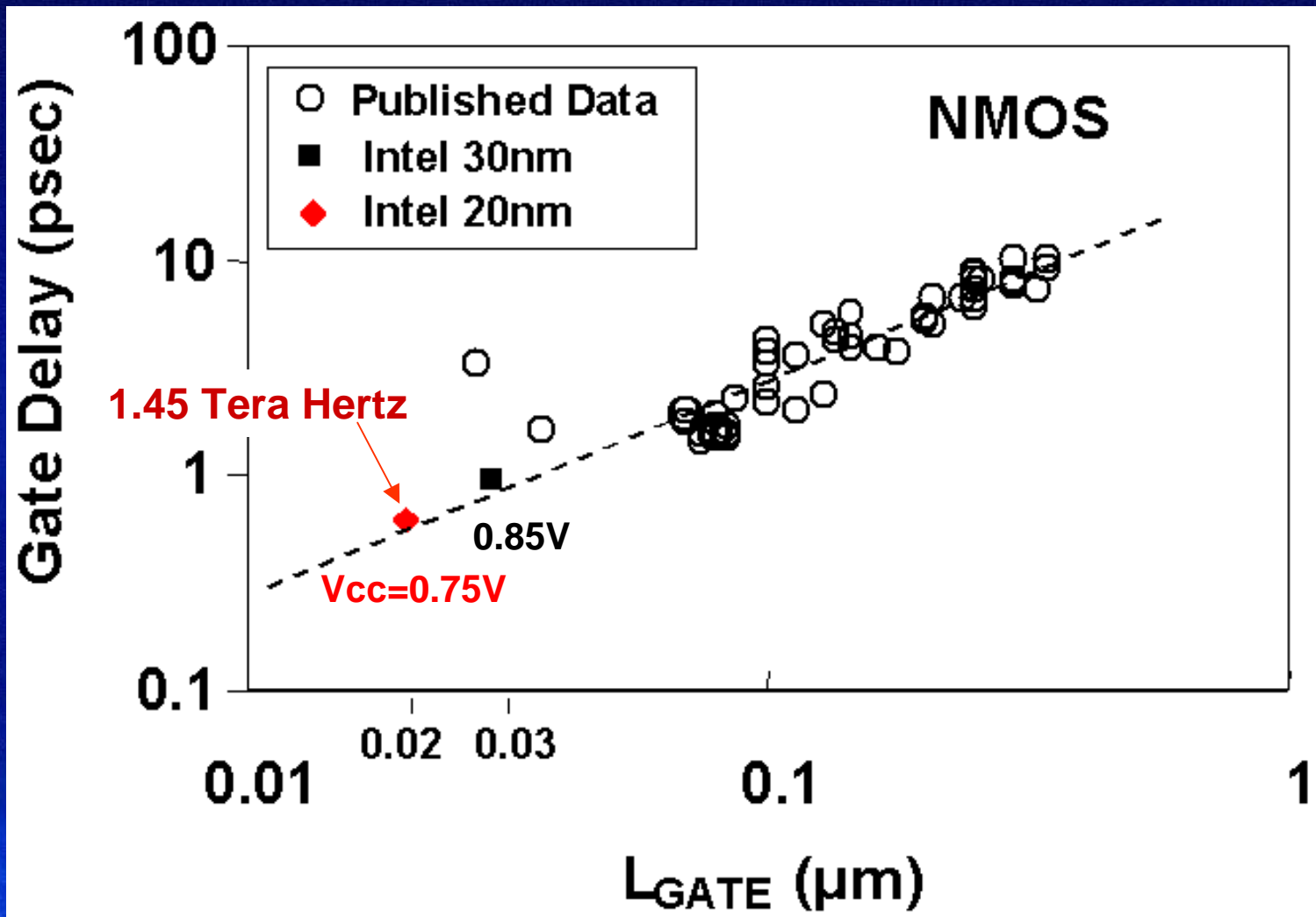




# Gate Delay & Drive Current

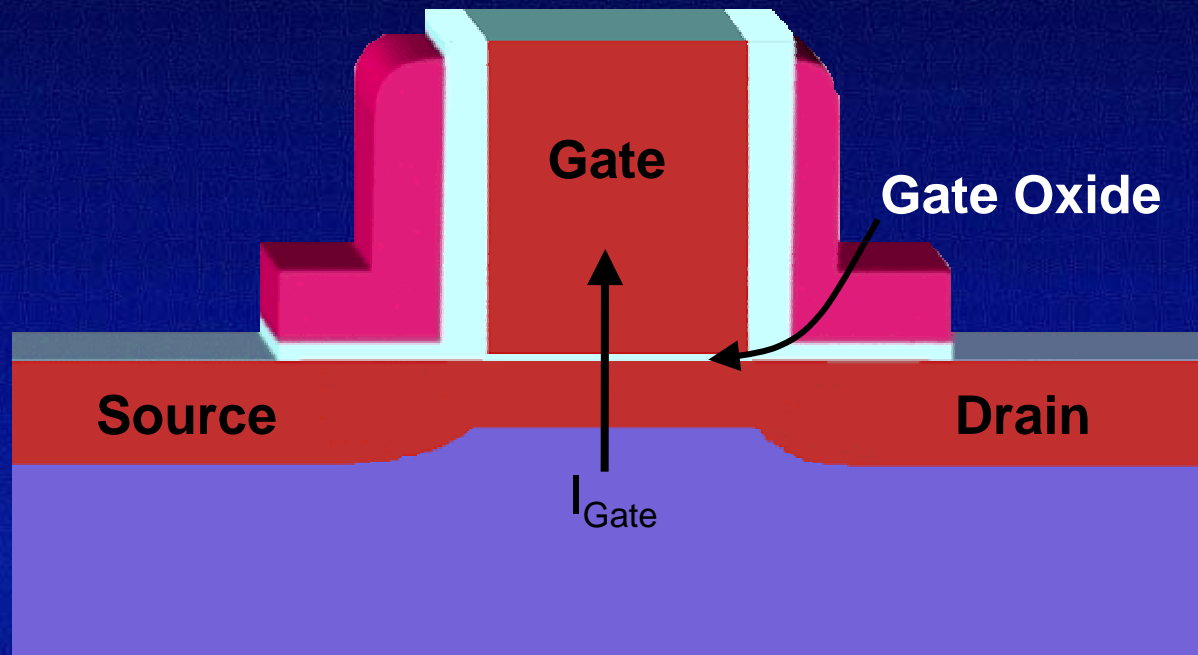
- Gate delay is the time it takes for current to travel from the source to the drain (across the channel).
- Drive current is the amount of current that flows when the transistor is turned on.
- Smaller gate delay and larger drive current translates into **FASTER** transistors and circuits.

# Intel Has Demonstrated the World's Fastest and smallest Transistors





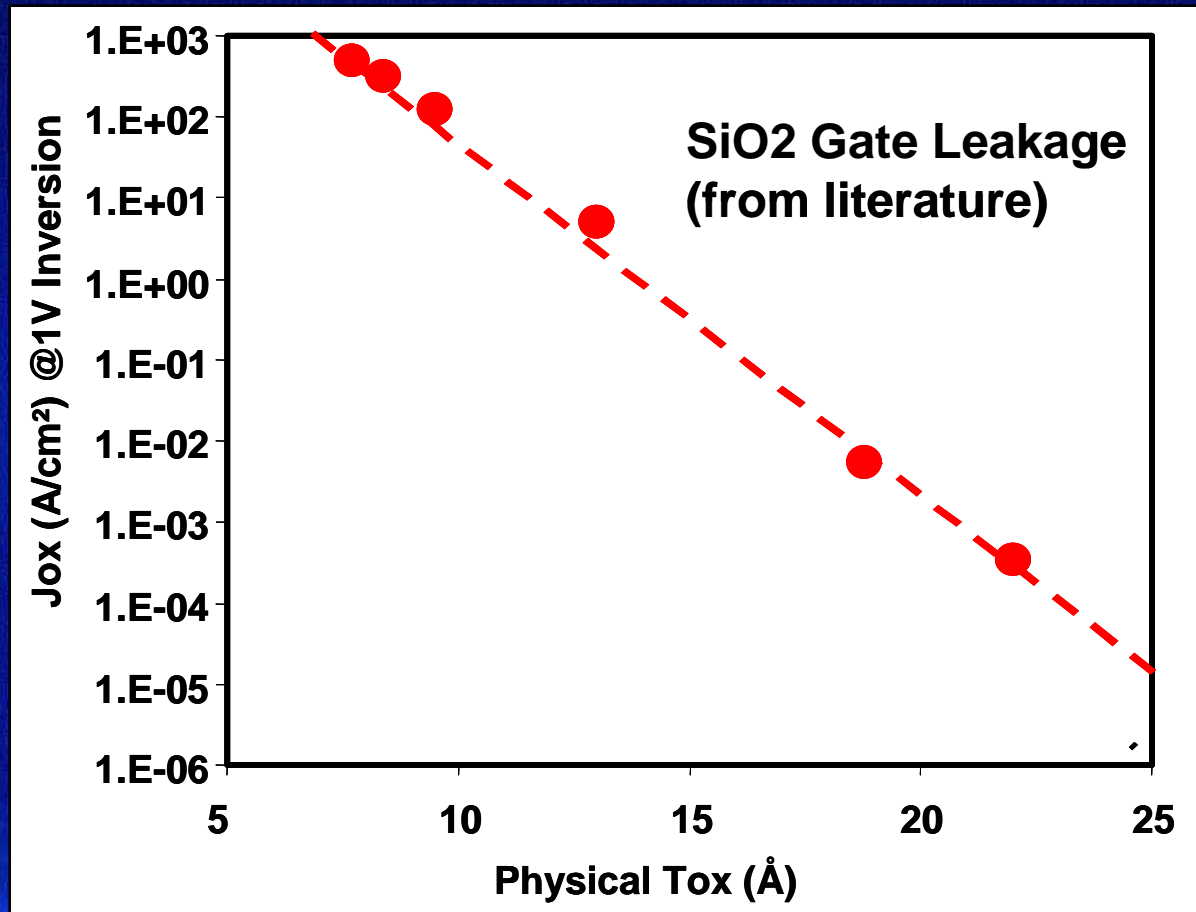
# Challenges: Gate Leakage



## Gate Leakage Current:

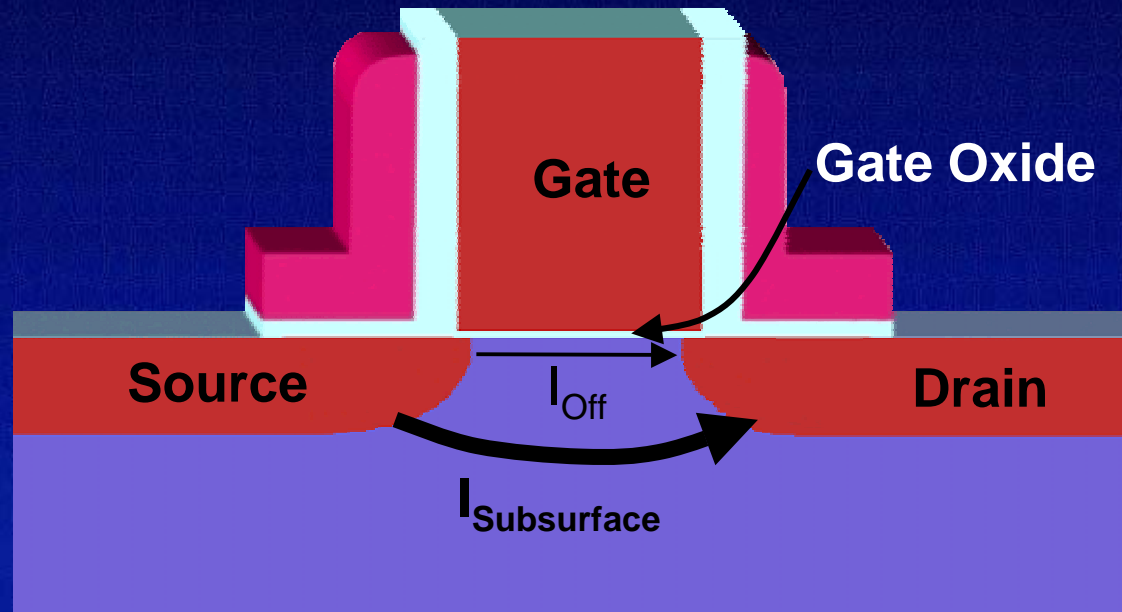
- Thinner gate oxides produce faster transistors
- We have reached the limit of Gate Oxide ( $\text{SiO}_2$ ) scaling.
  - 30nm transistor had 0.8nm gate oxide
- Thinner oxides leak more.
  - Gate oxide can get so thin it no longer acts as a good insulator

# Thin Gates have More Leakage



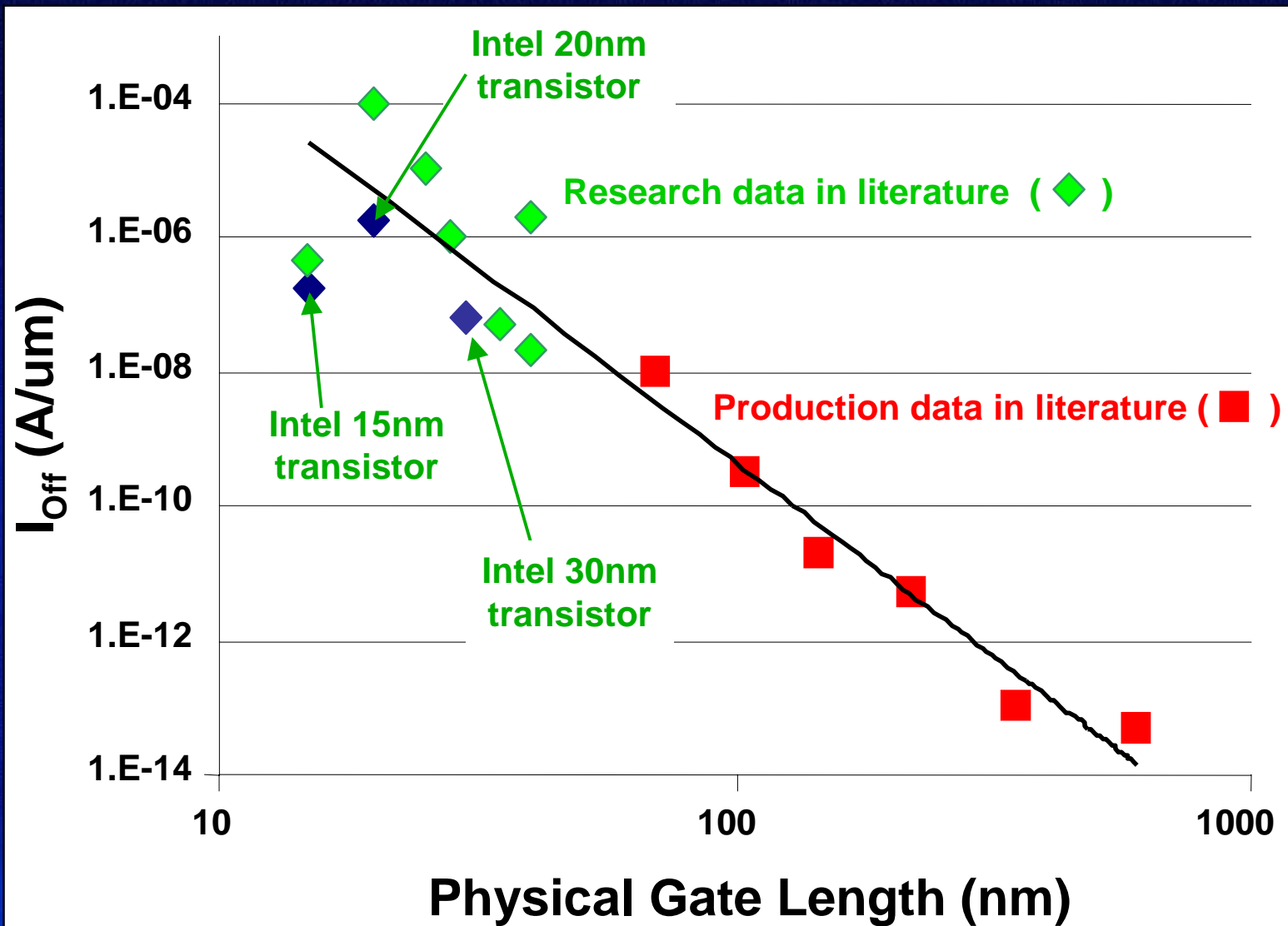


# Challenges: Off-state Leakage



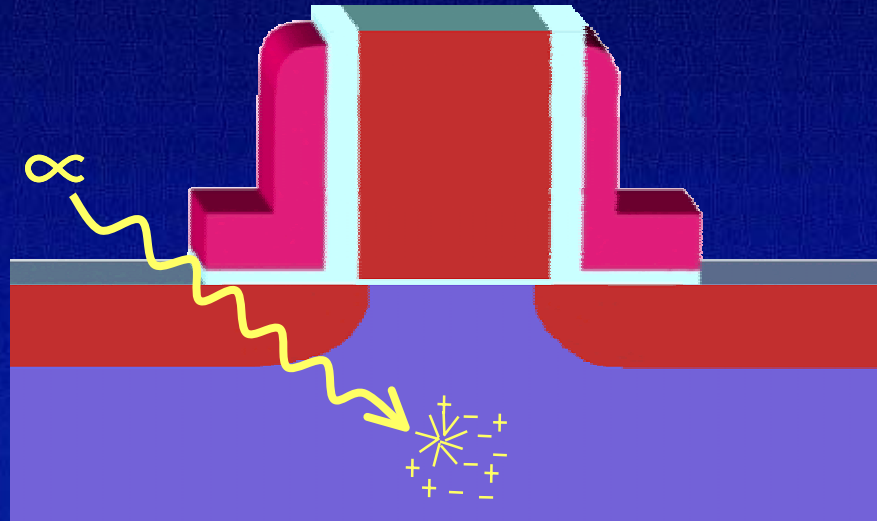
## Off-state (Sub-threshold) leakage:

- Ideally, current only flows across the channel (directly beneath the gate) from source to drain when the transistor is turned on.
- If current flows under the channel when the transistor is turned off, it is called Off-state (or Sub-threshold) leakage.
- Sub-threshold leakage consumes power in the standby or off state.
- A leaky device requires a higher operating voltage





# Soft Error Rate



- Alpha particles (from atmosphere or package) strikes silicon
- Impact causes ionization of charge carriers
- This unexpected charge can cause a 'soft error' in the logic or memory cells
- Smaller transistors are more susceptible to soft errors



# Solutions

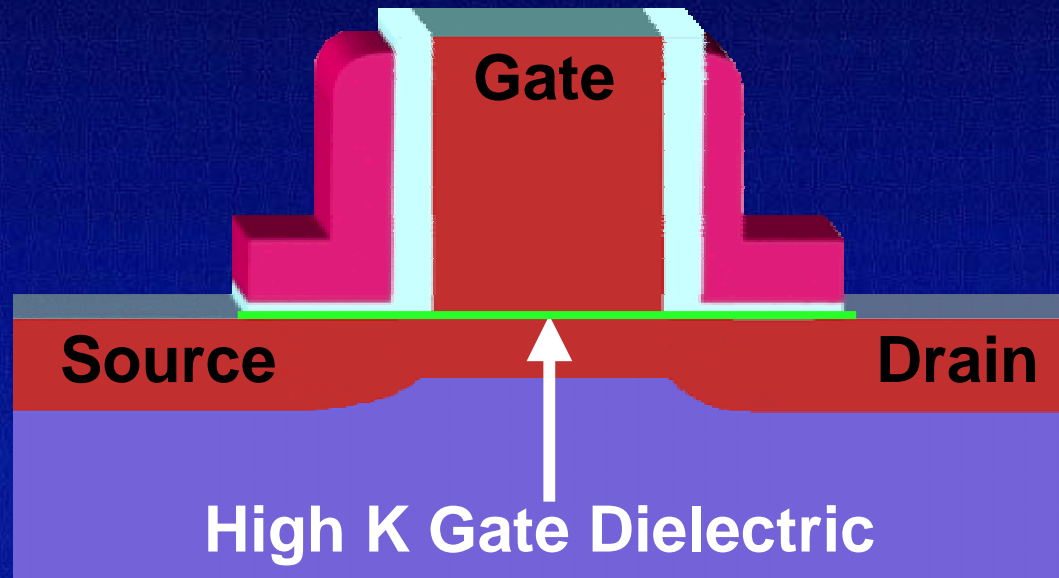
## TeraHertz Transistors

### Intel's New Transistor Architecture

- Depleted Substrate Transistor (DST)  
With Raised source and drain
- High-K gate dielectrics
- Low voltage operation



# High K Gate Dielectric



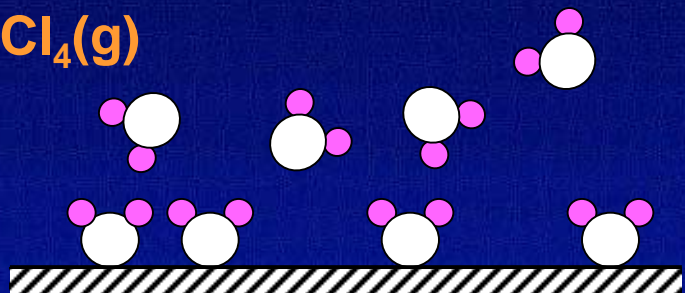
## High K dielectric

- New material replaces  $\text{SiO}_2$
- Thicker physical film but same capacitance
- 10,000x lower gate leakage current for same capacitance

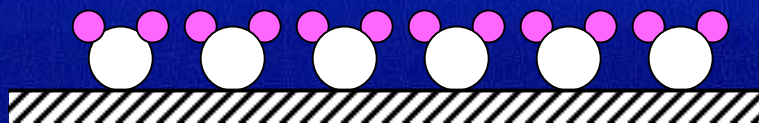


# High-K Gate Dielectric Formed Using Atomic Layer Deposition

$\text{ZrCl}_4(\text{g})$

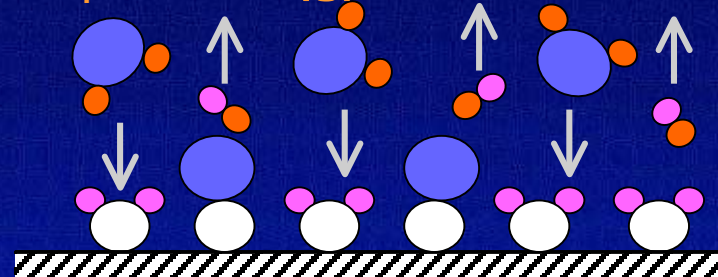


Step 1

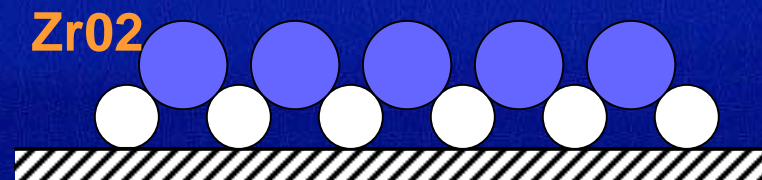


Step 2

$\text{ZrCl}_4 + 2\text{H}_2\text{O}(\text{g}) \rightarrow \text{ZrO}_2 + 4\text{HCl}(\text{g})$



Step 3

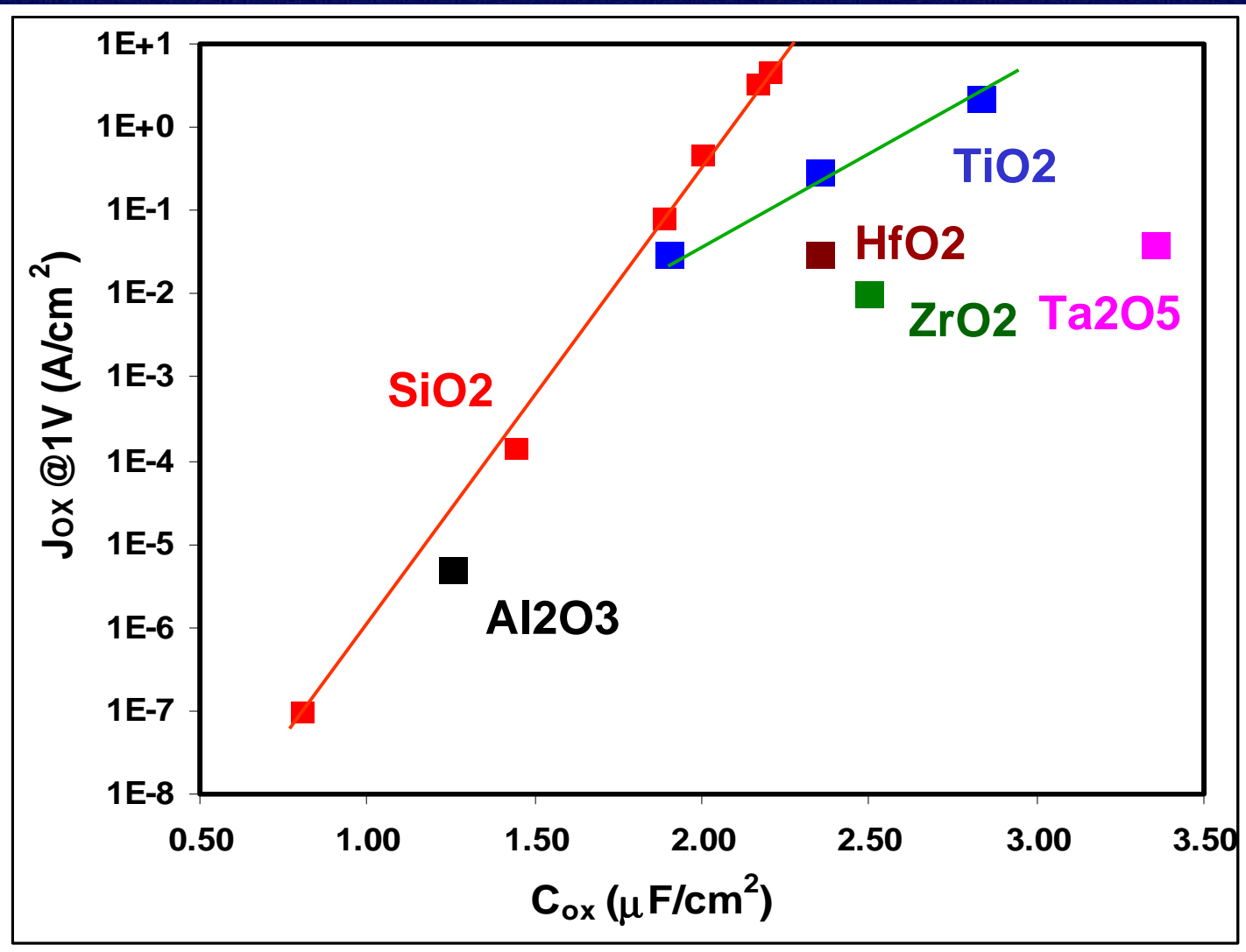


Step 4

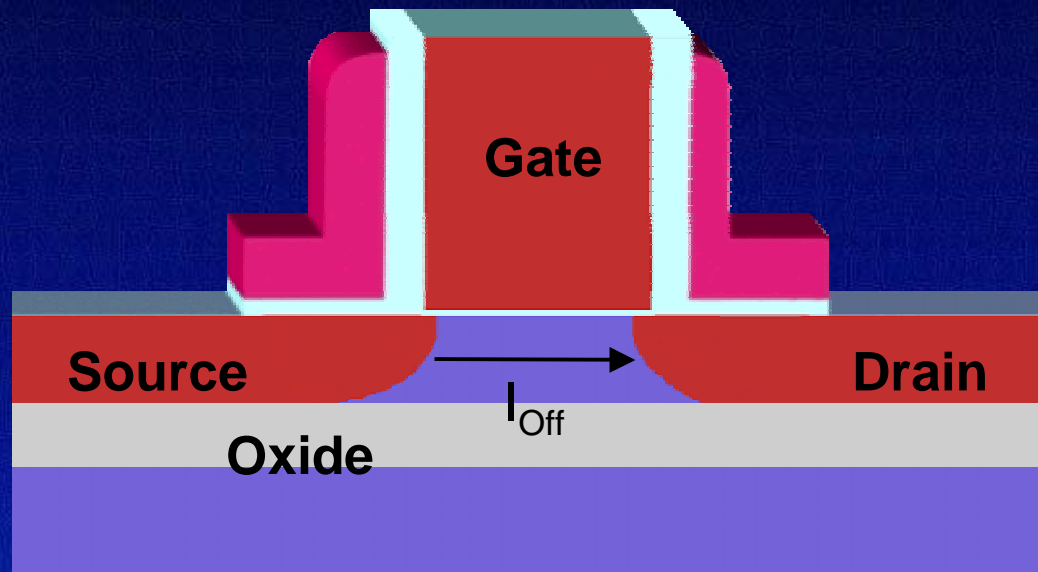
- Sequential introduction of precursors  $\text{ZrCl}_4(\text{g})$ ,  $\text{H}_2\text{O}(\text{g})$
- Surface reaction between substrate & each precursor until saturation



# Alternative Gate Dielectrics to Reduce Gate Leakage



# Ultra Thin Body SOI



## Benefits

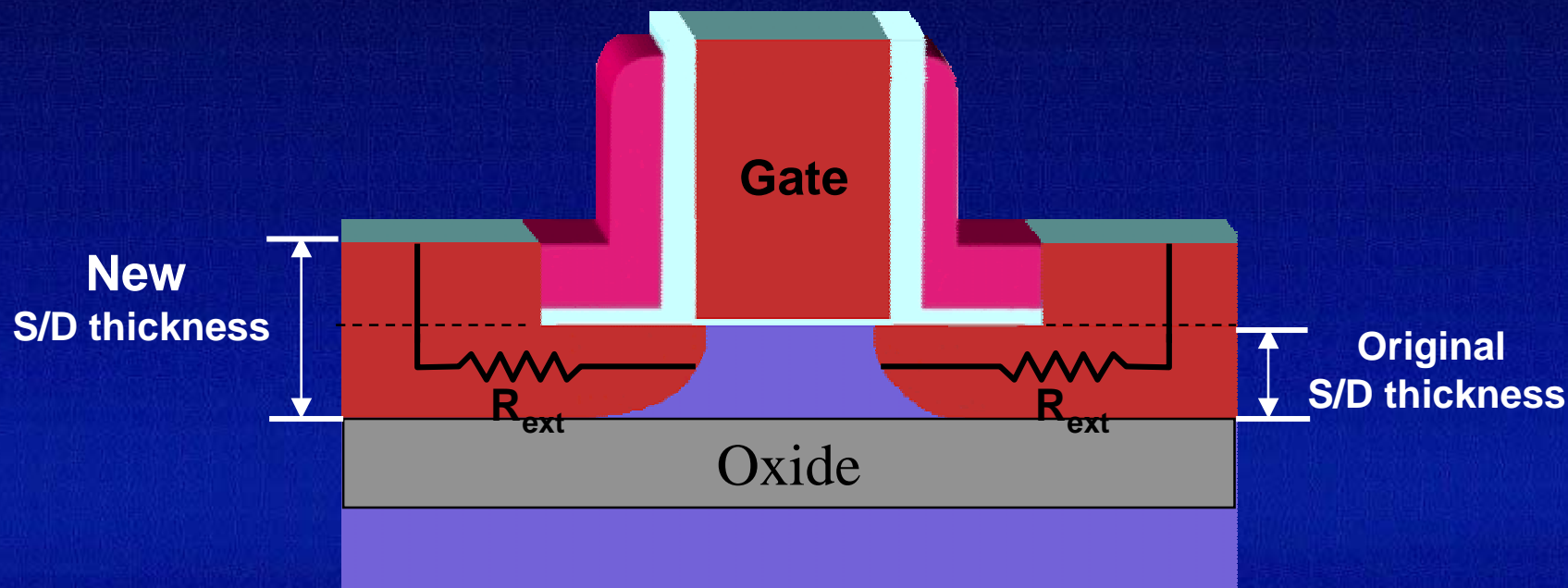
- No leakage path through substrate
- Lowest junction capacitance
- Less voltage required to turn on transistor
- No floating body effect

## Negative

- High resistance in Source/Drains



# Depleted Substrate Transistor

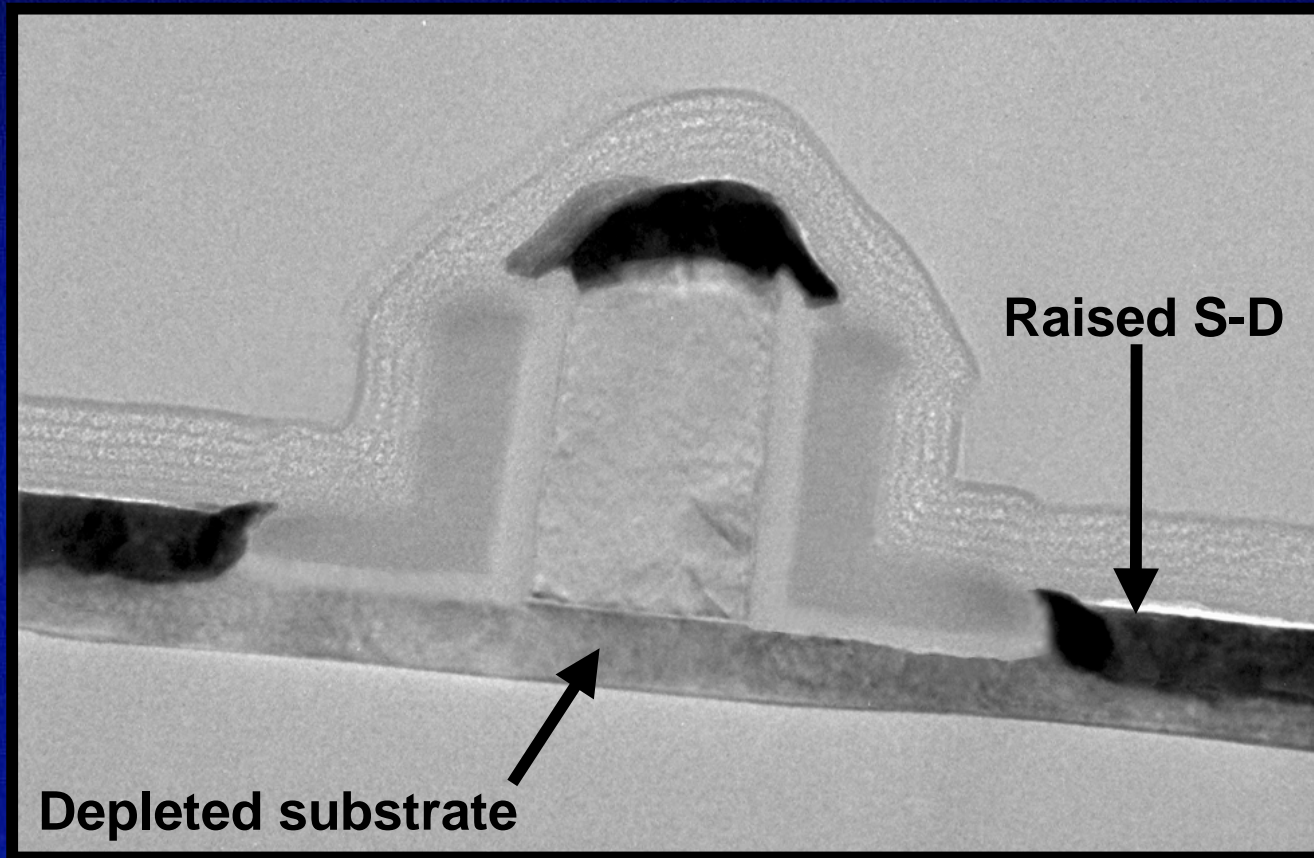


## Ultra Thin SOI plus Epitaxy Grown Source Drain

- Decreases resistance
- Higher drive current
- No increase in junction capacitance

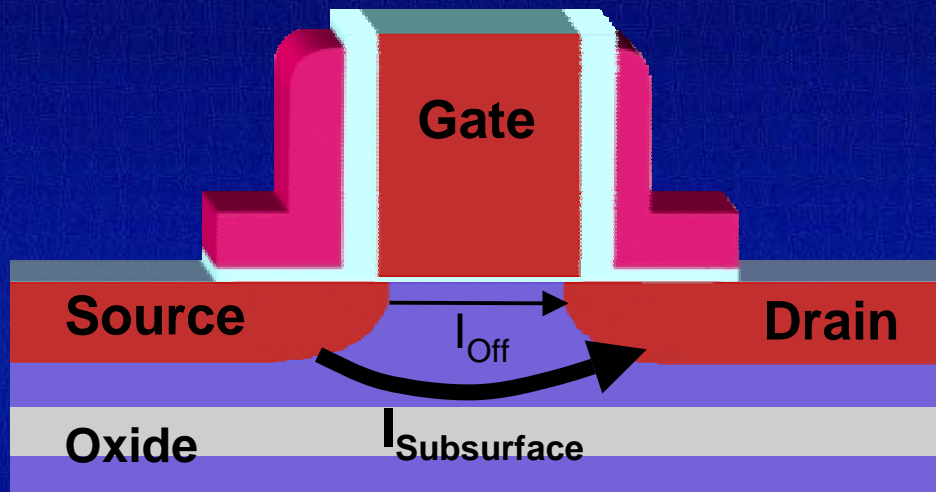


# Raised Source-Drains Combined with Depleted Substrate

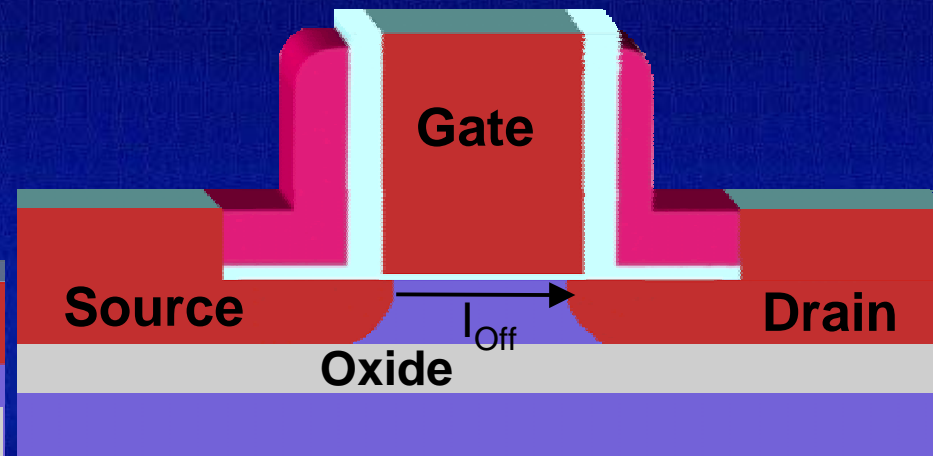




# DST Eliminates Leakage Paths Through Substrate



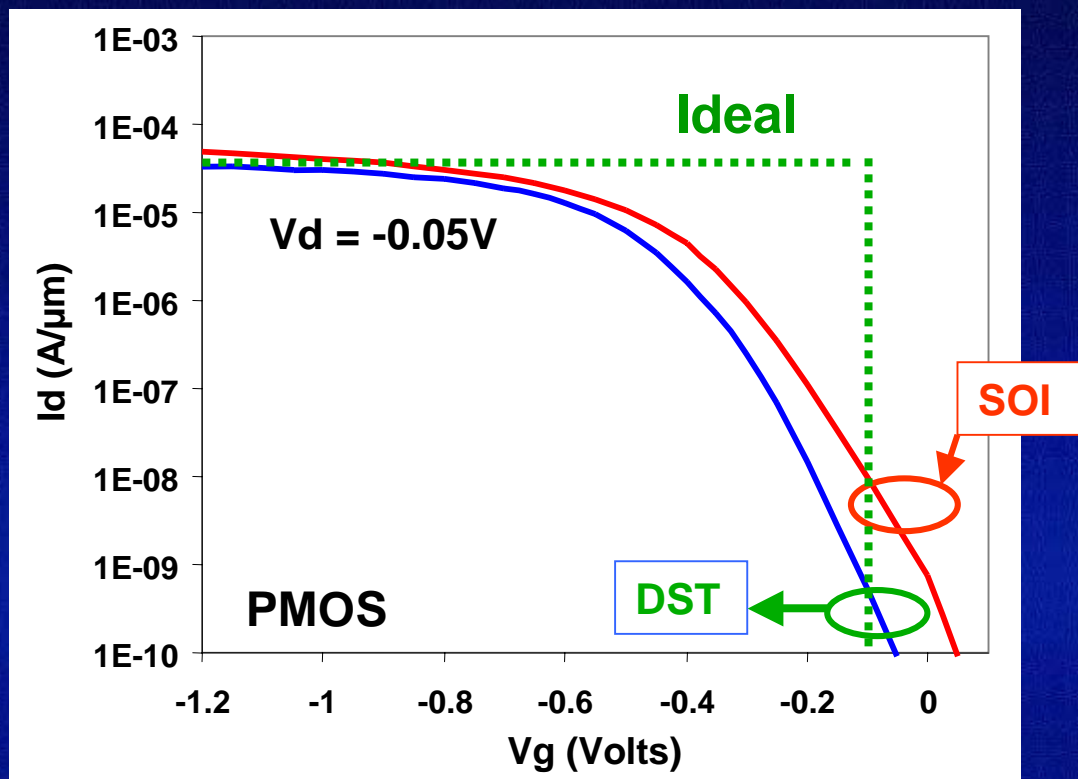
**Partially Depleted SOI**



**DST**

PD SOI has same  $I_{\text{off}}$  performance as bulk Silicon

# DST Outperforms PD SOI

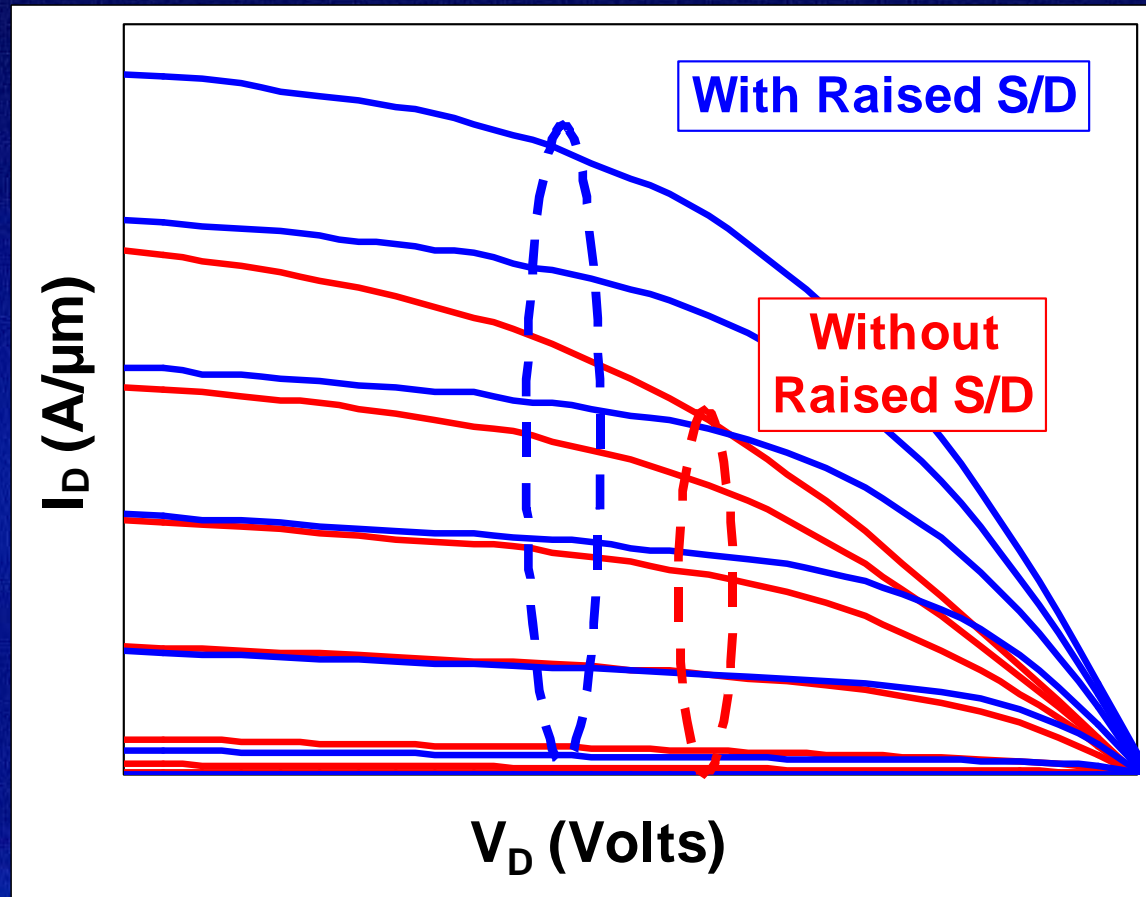


- DST achieves much steeper sub-threshold slope and lower  $I_{\text{off}}$  than both SOI and bulk Si

- Up to 100x lower leakage than partially depleted SOI !

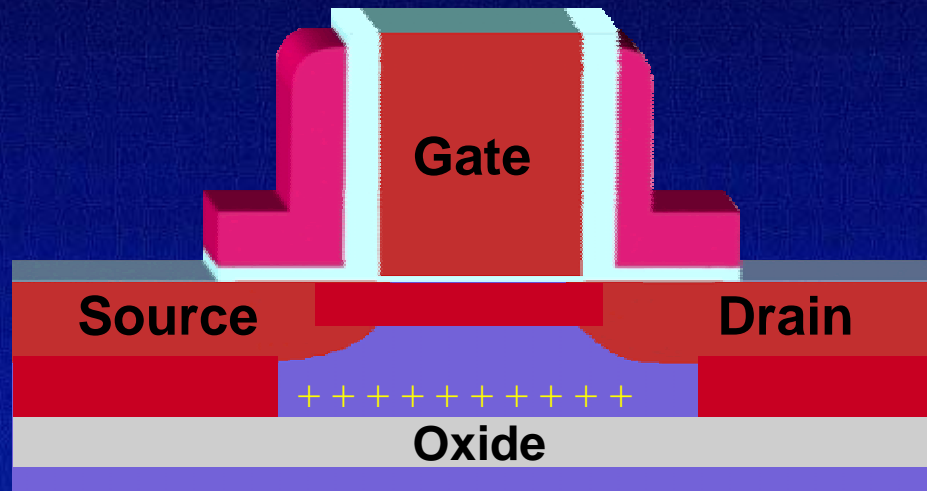


# Raised Source and Drain Reduces Parasitic Resistances and Improves $I_{D,SAT}$



30% increase in drive current!

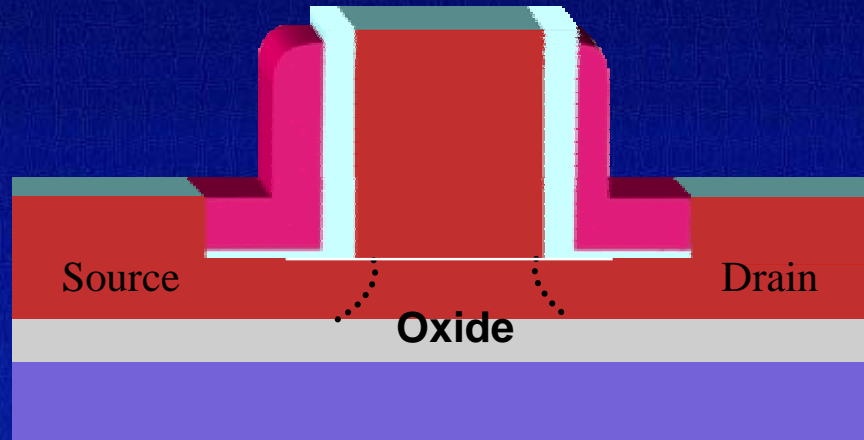
# Floating Body Problem with PD SOI



- Transistor Current creates charge below channel
- Charge collects causing voltage on silicon body to rise or 'float'
- Transistor  $V_t$  depends on previous state

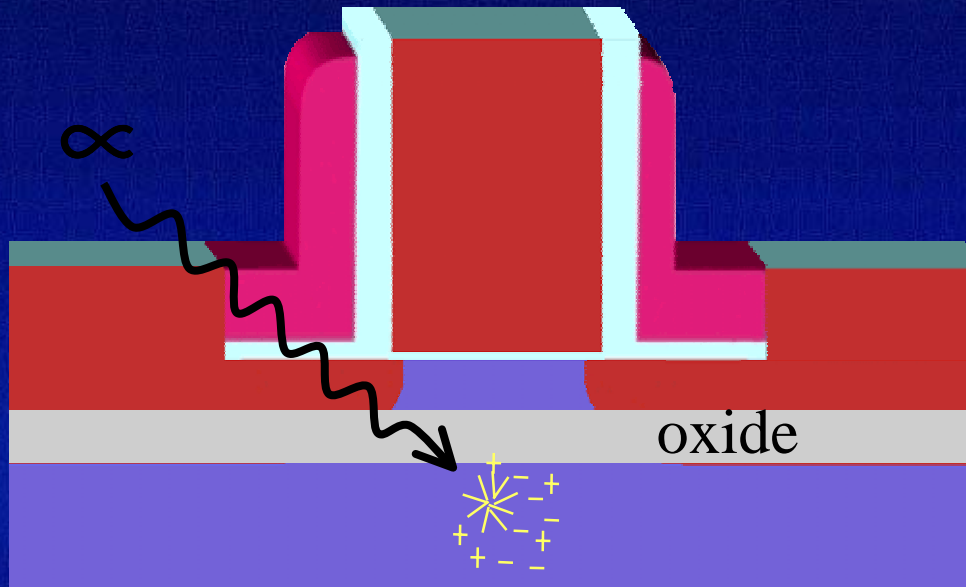


# DST Eliminates Floating Body Effect



- Silicon channel is fully depleted during operation of DST transistors
  - No chance for charge build up
- No design changes required for DST!

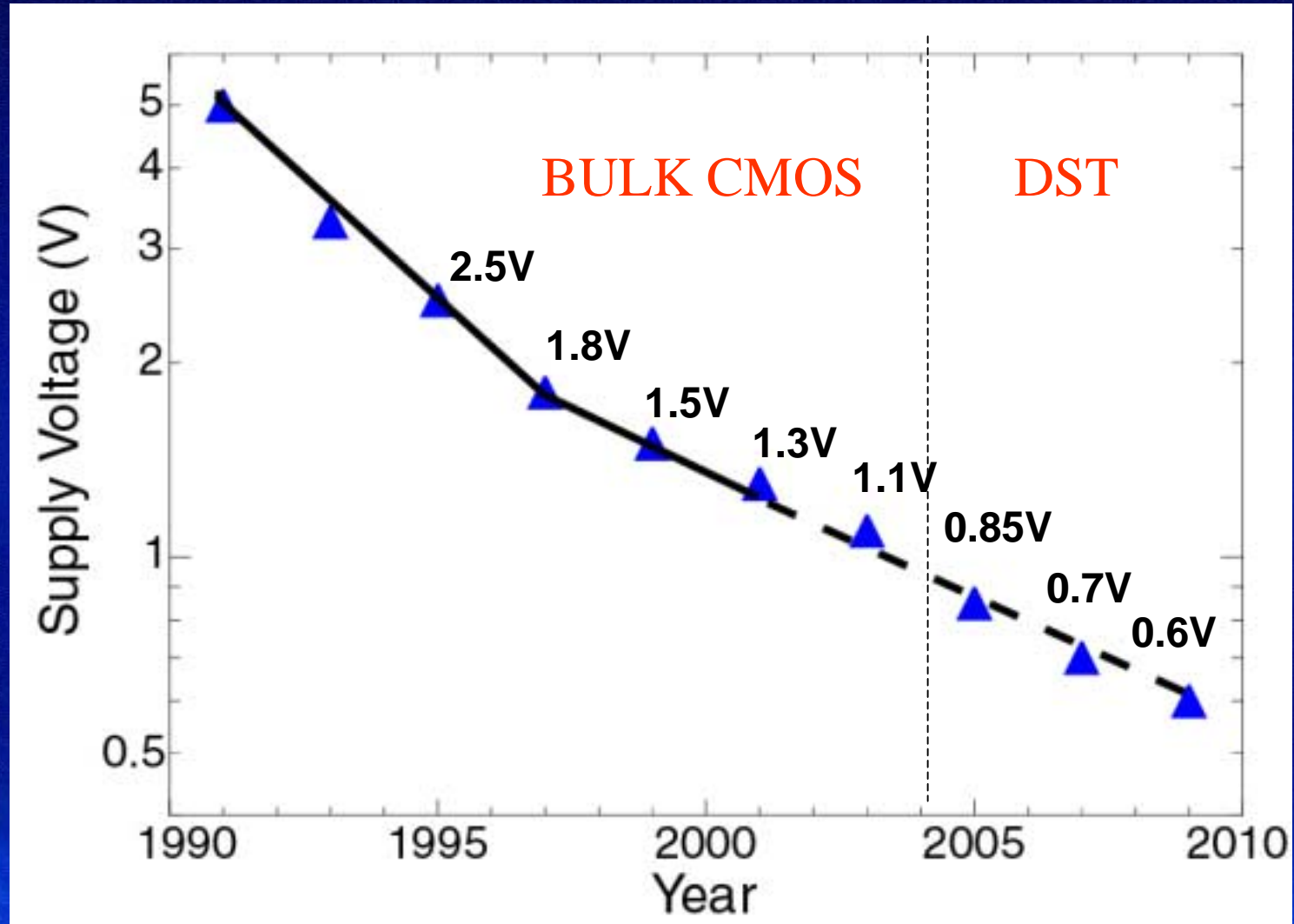
# DST Minimizes Soft Error Rate



- Alpha particles are absorbed deep into silicon where impact causes ionization of charge carriers
- Transistor is isolated from carriers by the buried oxide insulator
- Expect substantial improvement in soft error rates with DST



# DST Enables Future Voltage Scaling

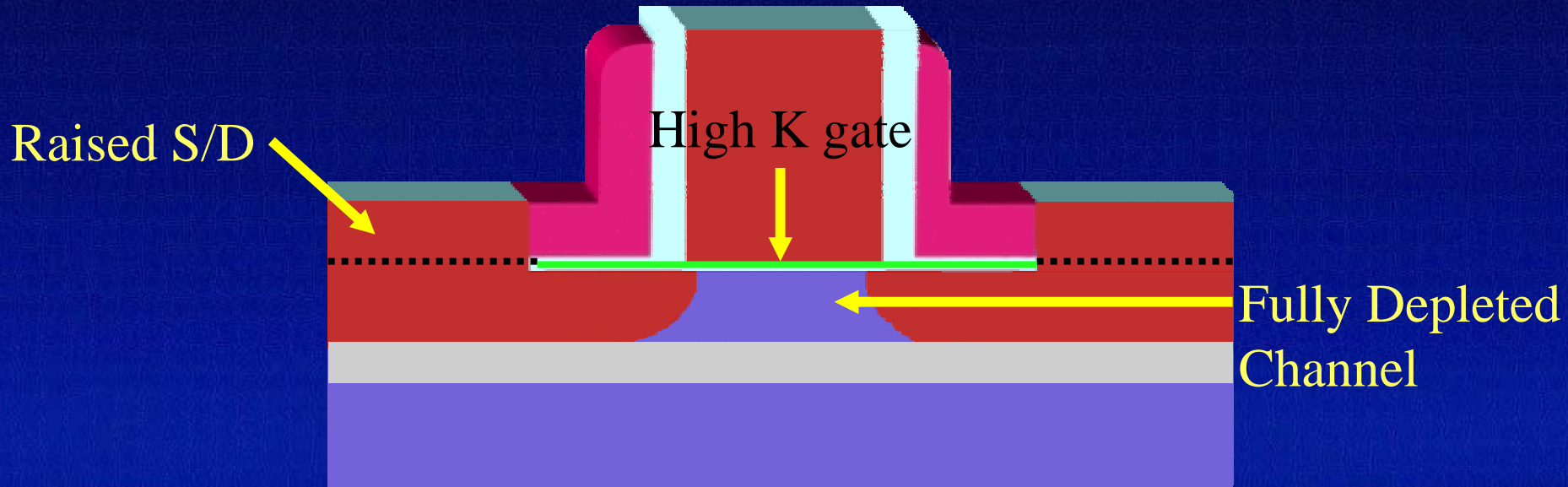


# Transistor Performance Comparison

	<u>Bulk</u>	<u>PD SOI</u>	<u>DST</u>
Si on Oxide Layer	NA	~100nm	<30nm
Raised source-drain	No	No	Yes
• Junction capacitance	Low	Lower	✓ Lowest
• Off state leakage	Low	Lower	✓ Lowest
• Soft error rate	Low	Lower	✓ Lowest
• Undesired floating body	No	Yes	✓ No
• Operating voltage	1.0x	1.0x	✓ 0.8x
• Gate delay	1.0x	0.9x	✓ 0.7x



# TeraHertz Transistor Architecture



- Eliminates subsurface leakage
- Solves high resistance
- Minimizes gate leakage
- Eliminates floating body effect
- Minimizes soft error rates
- 50% lower junction capacitance than PD SOI



# Conclusions

## **We have defined a new transistor architecture**

- Terahertz operation
- Low power consumption
- Scalable beyond 65nm technology node

## **All of the key elements have been demonstrated**

- New transistor structure
  - DST with raised source drain
- High k gate dielectric
- 30nm, 20nm, & 15nm CMOS gate length
- Terahertz operation at 0.75V



# Terahertz Transistor Schedule

- Intel's most advanced development and manufacturing capability is on 300mm wafers
  - Advanced lithography
  - High K dielectrics
  - Raised source-drains
  - Depleted Substrate Transistors
- We believe that TeraHertz transistor architecture will become the clear choice for the second half of the decade.



# Back-up information



# Intel Logic Papers at IEDM

- **Gasser: 300mm manufacturing**
  - Lowest cost manufacturing
- **Thompson: Px60 60nm transistors**
  - best transistor in manufacturing
- **Chau: Depleted Substrate Transistors**
  - New architecture and best performance/power at 50nm gate length
- **Chau: High frequency measurements of high K transistors**
  - Best performance with high k gates
- **Garcia: Transistor CAD model**
  - Hard core device physics